The Phase Stabilities of the Servo Circuit in a Rubidium Vapor Cell Frequency Standard

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Abstract: This paper mainly discusses the phase stabilities of a T-type frequency selector and RC phase-shift circuit which are used in the servo circuit of a rubidium vapor cell frequency standard, and analyses the mechanism how the additional phase variations which come from the two circuits influence the frequency stability of the rubidium standard. We present a new method of realizing a digital phase shifter based on CPLD(Complex Programmable Logic Device) for the synchronous detection reference signal. In comparison with traditional RC phase shifter, this method has many advantages such as good phase stability, high precision of phase shift and convenience for phase adjustment. It has been applied in a miniature rubidium frequency standard of our laboratory.

Key words: rubidium vapor cell frequency standard, phase stability, servo circuit, CPLD, digital phase shifter

INTRODUCTION

The servo circuit is a critical module of the vapor cell rubidium frequency standard. The frequency selector, synchronous phase detector, phase shifter, modulation oscillator and integrator that completed the servo circuit are shown in Figure 1. The frequency offset caused by the circuits after the synchronous phase detector can be corrected through the servo loop. However, the frequency offset caused by the circuits before the synchronous phase detector (including itself) is equivalent to the noise of the physics package, which is impossible to be corrected by the servo loop and will degrade the output frequency stability. This paper mainly concerns how the phase fluctuation of the circuits before the synchronous phase detector (including itself) influences the output frequency stability.

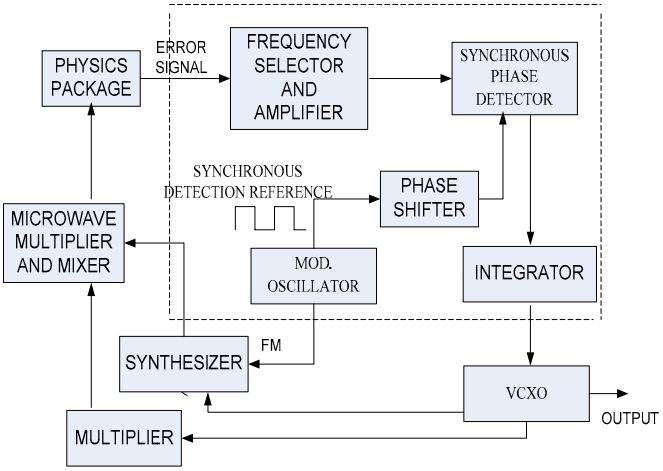

Figure 1: The block diagram of a rubidium frequency standard

THE ANANYSIS OF THE ADDITIONAL PHASE VARIATIONS

The low frequency sine wave modulation signal is set to be

$$S_m = A_m \sin(\omega_m t) \qquad (1)$$

wher ω_m is the modulation angular frequency and A_m is the amplitude of modulation. The fundamental component of the frequency discrimination signal may be approximately expressed as

$$S_L = B_s \sin(\omega_m t + \phi + \phi_1) \qquad (2)$$

where ϕ is dependent on the difference between ν' the center frequency of the

microwave excitation and ν_0 the frequency of the atomic reference, ϕ_1 is the phase offset caused by the mixer circuit and physics package, and B_s is a factor related to the discrimination feature of the physics package. After passing a frequency selector and amplifier, the output signal is written as

$$S_A = K_a B_s \sin(\omega_m t + \phi + \phi_1 + \phi_2) \qquad (3)$$

where ϕ_2 is the phase offset caused by the frequency selector and K_a describes the gain of the amplifier. As the synchronous phase detector is a multiplier, from (1) and (2), the output signal of the phase detector is given by

$$S_P = K_a K_p B_s \sin(\omega_m t + \phi + \phi_1 + \phi_2)\sin(\omega_m t)$$

$$= (-1/2) K_a K_p B_s [\cos(2\omega_m t + \phi + \phi_1 + \phi_2) - \cos(\phi + \phi_1 + \phi_2)] \quad (4)$$

with K_p being a parameter introduced by the phase detector.

The AC component is filtered through an integrator and one gets the output to VCXO as a control voltage variable

$$\triangle V_c = (1/2) K_a K_p B_s \cos(\phi + \phi_1 + \phi_2) \qquad (5)$$

In the ideal condition, $\phi_1 + \phi_2 = 0$ and $\phi = 90°$, when $\nu' = \nu_0$, then $\triangle V_c = 0$ and output frequency is locked to ν_0. But in the actual situation $\phi_1 + \phi_2 \neq 0$, when $\phi + \phi_1 + \phi_2 = 90°$, it leads to $\triangle V_c = 0$ and $\nu' \neq \nu_0$, thus the output frequency is locked to an offset from ν_0. For this reason, a phase shifter is inserted before the synchronous phase detector to correct the phase offset, so that

$$\triangle V_c = (1/2) K_a K_p B_s \cos(\phi + \phi_1 + \phi_2 + \phi_3) \qquad (6)$$

where ϕ_3 is the phase shift of the phase shifter and one sets $\phi_1 + \phi_2 + \phi_3 = 0$. So when $\nu' = \nu_0$, we have $\triangle V_c = 0$, then output frequency is locked to ν_0.

In fact, because the value of $\phi_1 + \phi_2 + \phi_3$ always depends on variations of the environmental temperature, the power supply and modulation frequency, it will fluctuate around zero.

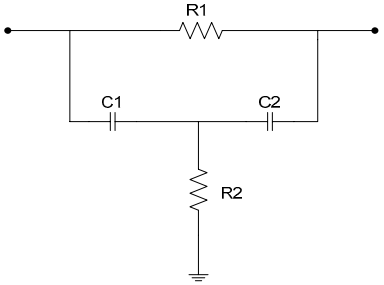

Figure 2: A simple T-type frequency selector

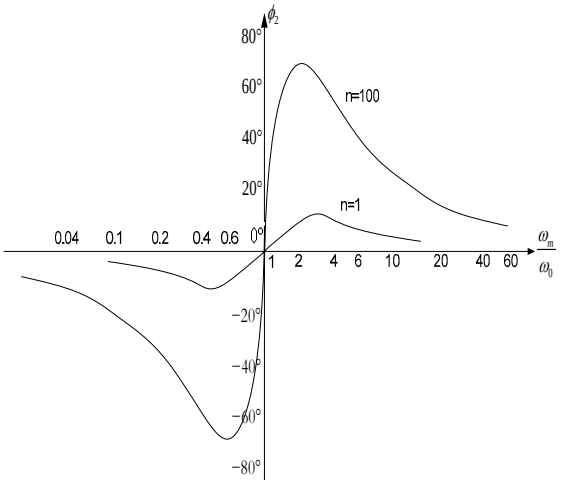

Figure 3：Phase-frequency response of the T-type frequency selector

The fluctuation of ϕ_2 stems from the

fundamental frequency selector. A classical T-type frequency selector is shown in Figure 2 and its phase-frequency response is shown in Figure 3. Obviously, the fluctuation of ϕ_2 is relative to the following factors:

i） The extent how much ω_m deviates to ω_0 (the resonant frequency of the T-type frequency selector), namely the stability of ω_m.

ii） The Q of the frequency selector, namely the amount of 'n'. For a fixed value of ω_m / ω_0, the phase shift is in proportion to the amount of 'n'. (Figure 3)

iii） The resonant frequency stability of the T-type frequency selector.

Some methods will be available to decrease the fluctuation of ϕ_2:

a） Improving the stability of ω_m by generating the modulation signal from VCXO directly.

b） Selecting the smaller value of 'n' in the condition of meeting the requirement of frequency selection.

c） Choosing the RC component with small temperature coefficient to ensure the stability of ω_0.

The fluctuation of ϕ_3 is commonly relative to the temperature stability of the RC component in the phase shifter and the triggering errors of the shaping circuit after the phase shifter.

The servo amplifier circuits, although straightforward, require care in execution and component selection, since the system is a frequency lock loop and offsets directly cause frequency errors. [1]

A PHASE SHIFTER BASED ON CPLD

For reducing the fluctuation of ϕ_3, a phase shifter based on CPLD is proposed. The block diagram is shown in Figure 4 where *fre1* is the modulation signal, *fre2* is the synchronous detection reference signal, *2n* is the dividing ratio.

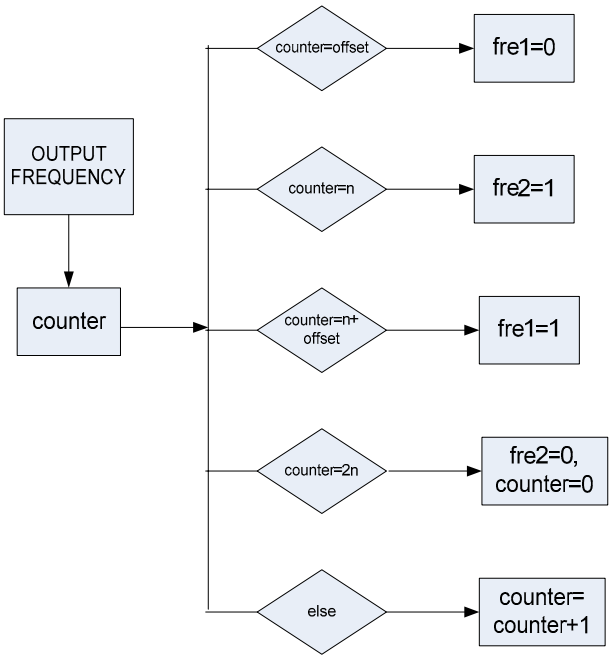

Figure 4: The block diagram of a digital phase shifter

As shown in Figure 4, *fre1* and *fre2* are the frequency division of VCXO by using a same counter, and the phase between *fre1* and *fre2* can be adjusted through modifying the value of *offset*. For output frequency f=10 MHz, and ω_m =160π, the minimal value of the phase shift $\varphi_{\min}$ is:

$$\varphi_{\min} = \omega_m / f = 8 \times 10^{-6} \times 2\pi$$

Obviously, it is a high precision phase shifter which can compensate the phase shift of φ_1 and φ_2, so the output frequency is locked to ν_0 accurately. Because *fre1* and *fre2* are obtained from VCXO, they have almost the same frequency stability and phase stability as VCXO which are nearly independent to the temperature and power fluctuations, so it is beneficial to the stability of φ_2 and φ_3 which influence the stability of output frequency.

The program below describes how to realize the digital phase shifter in a CPLD by Verilog HDL.

```
module phaseshifter(clk, fre1,fre2);
    input clk;
    output fre1,fre2;
    parameter offset,n;
    reg fre1,fre2;
    reg [m:0] counter;
    always@(posedge clk )
    begin
    if(counter==offset)
    begin
      fre1<=0;
      counter<=counter+1;
    end
    else if(counter==n)
    begin
      fre2<=1;
      counter<=counter+1;
    end
    else if(counter==n+offset)
    begin
      fre1<=1;
      counter<=counter+1;
    end
    else if(counter==n+n)
    begin
      fre2<=0;      counter<= 1;
    end
    else
    begin
      counter<=counter+1;
    end
        end
endmodule
```

CPLDs are a class of programmable logic devices. They feature the speed and design simplicity. With CPLD, ω_m and 'offset' can be changed through a software easily. The digital phase shifter uses a little part of the resources of CPLD. Based on a CPLD, our laboratory has realized controlling unit, initialing the synthesis circuit, and producing a locking signal.

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